PATENT
Attorney Docket No.: 19427-004930US
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OWyatt

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Not Assigned
Todd C. Mowry	Art Unit: Not Assigned
Application No.:	
Filed: Herewith	PRELIMINARY AMENDMENT
For: PREFETCHING HINTS	

Assistant Commissioner for Patents
Washington, D.C. 20231

March 12, 2001

Sir:

Prior to examination of the above-referenced application, please enter the following amendments and remarks.

IN THE SPECIFICATION:

Please **replace** the paragraph beginning at **page 1, line 5**, with the following two paragraphs:

--This application is a Continuation of U. S. Application No. 08/982,244, filed December 1, 1997, which is a Continuation of U.S. Application No. 08/410,524, now U.S. Patent No. 5,732,242.

A preferred embodiment of the present invention is incorporated in a superscalar processor identified as "R10000," which was developed by Silicon Graphics, Inc., of Mountain View, California. Various aspects of the R10000 are described in commonly-owned copending patent applications having serial numbers: 08/324,124 ("Cache Memory"), 08/324,127 ("Redundant Mapping Tables"), 08/324,128 ("Memory Translation"), 08/324,129 ("Address Queue") and 08/404,625 ("Address Queue"), which are hereby incorporated by reference in their entirety for all purposes.--

Please **replace** the paragraph beginning at **page 8, line 18**, with the following rewritten paragraph:

--The addressing architecture for the system of Fig. 1 is illustrated in Fig. 2. Address information held in queue 22 (e.g., offset value and/or register numbers) is forwarded to an integer register file 1011 and address calculate unit 1012, which generates a virtual address (i.e., V[all]; a complete virtual address) on line 1014. This virtual address is converted to a